WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a gate electrode, having side surfaces, over an upper surface of a substrate with a gate dielectric layer therebetween;

an oxide liner on the side surfaces of the gate electrode and the upper surface of the substrate;

a nitride liner on the oxide liner; and

a sidewall spacer on the nitride liner.

2. The semiconductor device according to claim 1, wherein:

the oxide liner comprises silicon oxide;

the nitride liner comprises silicon nitride; and

the sidewall spacer comprises a silicon oxide, silicon nitride or silicon oxynitride.

3. The semiconductor device according to claim 2, wherein the sidewall spacer comprises a silicon oxide.

4. The semiconductor device according to claim 3, wherein the silicon oxide sidewall spacer has a dielectric constant (k) no greater than about 3.9.

5. The semiconductor device according to claim 2, comprising shallow source/drain extensions in the upper surface of the substrate on each side of the gate electrode under the sidewall spacer.

6. The semiconductor device according to claim 5, wherein the source/drain extensions contain a P-type impurity.

7. The semiconductor device according to claim 6, wherein the P-type impurity comprises boron.

8. The semiconductor device according to claim 7, wherein the shallow source/drain extensions have a junction depth ($X_j$) of about 200 Å to about 300 Å.

9. The semiconductor device according to claim 2, wherein:

the oxide liner has a thickness of about 10 Å to about 50 Å; and

the nitride liner has a thickness of about 50 Å to about 200 Å.

10. A method of manufacturing a semiconductor device, the method comprising:

forming a gate electrode, having side surfaces, over an upper surface of a substrate with a gate dielectric layer therebetween;

forming a composite liner comprising:

an oxide liner on the side surfaces of the gate electrode and the upper surface of the substrate; and

a nitride liner on the oxide liner; and

forming a sidewall spacer on the composite liner.

11. The method according to claim 10, wherein:

the oxide liner comprises a silicon oxide;

the nitride liner comprises a silicon nitride; and

the sidewall spacer comprises a silicon oxide, silicon nitride or silicon oxynitride.

12. The method according to claim 11, comprising forming the sidewall spacer of a silicon oxide having a dielectric constant (k) no greater than about 3.9.

13. The method according to claim 11, comprising depositing the silicon nitride liner by decoupled plasma deposition at a temperature no greater than about 400°C.

14. The method according to claim 13, comprising depositing the silicon oxide liner by decoupled plasma deposition at a temperature no greater than about 400°C.

15. The method according to claim 13, comprising:

forming the silicon oxide liner at a thickness of about 10 Å to about 50 Å; and

forming the silicon nitride liner at a thickness of about 50 Å to about 200 Å.

16. The method according to claim 11, comprising ion implanting to form shallow source/drain extensions in the upper surface of the substrate, using the gate electrode as a mask, before forming the composite liner.

17. The method according to claim 16, comprising ion implanting a P-type impurity to form the source/drain extension.

18. The method according to claim 17, wherein the P-type impurity comprises boron.

19. The method according to claim 18, comprising forming the source/drain extensions at a junction depth ($X_j$) of about 200 Å to about 300 Å.